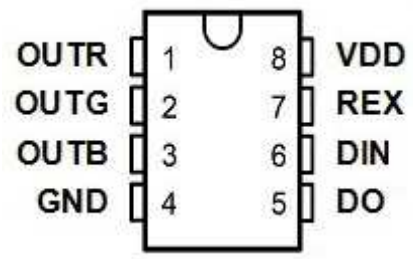
Description

P9823B is 3 channel LED driver control chip, internal integrated MCU digital interface, data latching, LED HV driver and so on circuit, it can through the peripheral controller to control 256 grayscale and Color dot luminescence of large outdoor screen by cascade control.

Feature

- The withstand voltage of output terminal is 17V
- Built-in VR-tube, the power terminal series resistance to VDD feet, without additional VR-tube
- Adjust grayscale circuit (can adjust 256 grayscale level)
- Built-in double RC oscillation, and clock synchronization according to the data signal line, cans automatically shaping forwarding follow-up data after undergoing the unit data.
- built-in power on reset circuit
- PWM control terminal can adjust 256 level, and scanning frequently >400Hz/s
- Series interface, cascade interface, it can completely receive and decode data through a single wire.
- When refresh rate is 30 frames/second, the cascade interface no less than 512 dot in low speed model, and the cascade interface no less than 1024 dot in high speed model.
- Data transmission speed is 800Kbps

Foot position



Leading –out terminal function:

No.	Symbol	Pin Name	Function Description
1	OUTR	LED output	Red PWM controller output
2	OUTG	LED output	Green PWM controller output
3	OUTB	LED output	Blue PWM controller output
4	GND	Ground	Connect to the ground

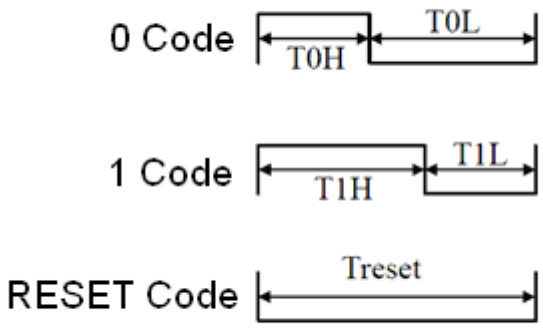
5	DOUT	Data output	Display the data cascade output
6	DIN	Data input	Display the data input
7	REX	External resistance	External resistance adjust current
8	VDD	Logic power	

Function

The chip uses the single communication mode, using zero code method to transmit the signal. After chip in the power on reset, Chip accept the data which DIN terminal send, when receive 24bit enough, DO terminal starts to forwarding data, to provide input data for the next chip. Before forwarding, DO has been pulled low. The chip will not accept new data, OUTR, OUTG, OUTB three PWM output terminals send corresponding signal ratio of different duty cycle based on 24bit data received, the signal cycle in 4ms. If the DIN input signal is the RESET signal, the chip will sent data which have received the data to the display, chip will accept new data after this data finished, transmitting data through the DO terminal after accept the original 24bit data, OUTR, OUTG, OUTB pin keep original output before receive RESET code, when receiving higher than t 24μs low level RESET code, the chip will output the 24bit PWM data pulse width to OUTR, OUTG, OUTB pin.

The chip adopts automatic shaping forwarding technology, makes the number of cascade is not limited by the signal transmission, limited only refresh speed. For example, we design a 1024 cascade, the refresh time is 1024X0.4X2 = 0.8192ms (chip data delay time is 0.4μs), there will be no flicker phenomenon.

Timing waveform

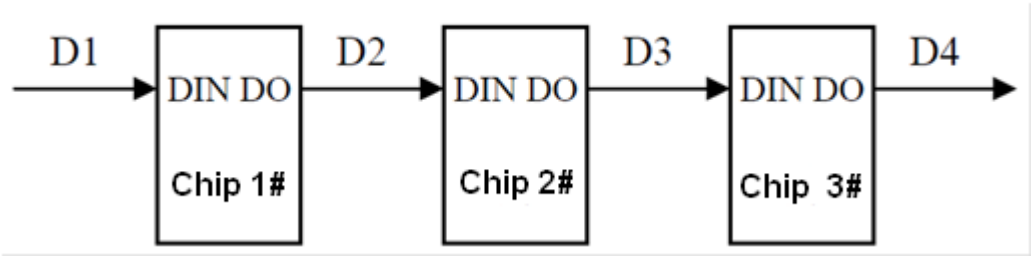


1）Input code pattern

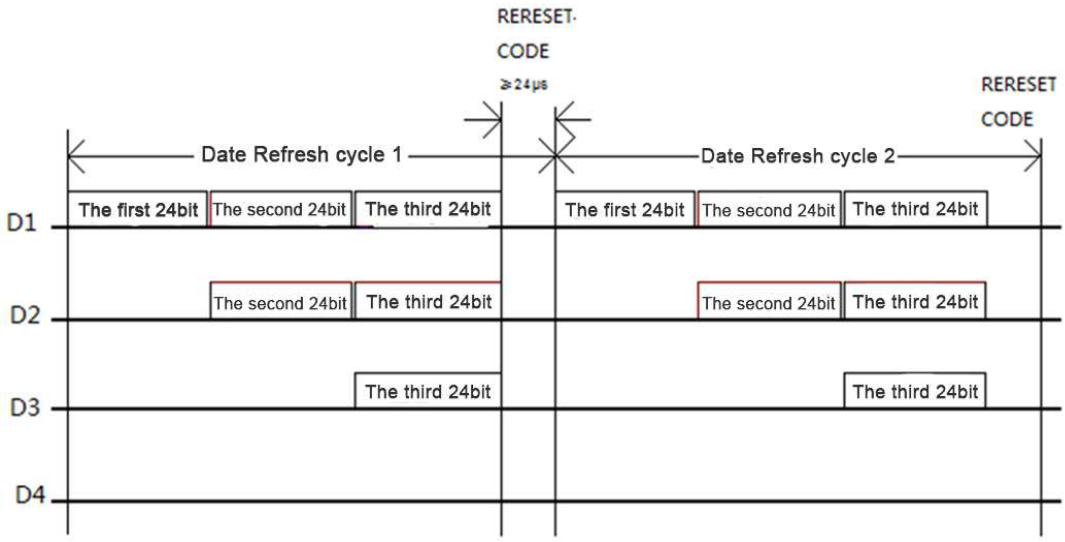
2）High speed mode time

Name	Description	Typically	Allowable error
T0H	0 code, high level time	0.35μs	±150ns
T1H	1 code, high level time	1.36μs	±150ns
T0L	0 code, low level time	1.36μs	±150ns
T1L	1 code, low level time	0.35μs	±150ns
RES	RESET code	50us	

3）Connect method



4）Data transmission method



Remark: D1 is the transmitted data of MCU; D2, D3, D4 as the data of cascade circuit automatic shaping forwarding data.

5）24bit data structure

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Remark: send the high bit at first, and send the data according to the RGB sequence